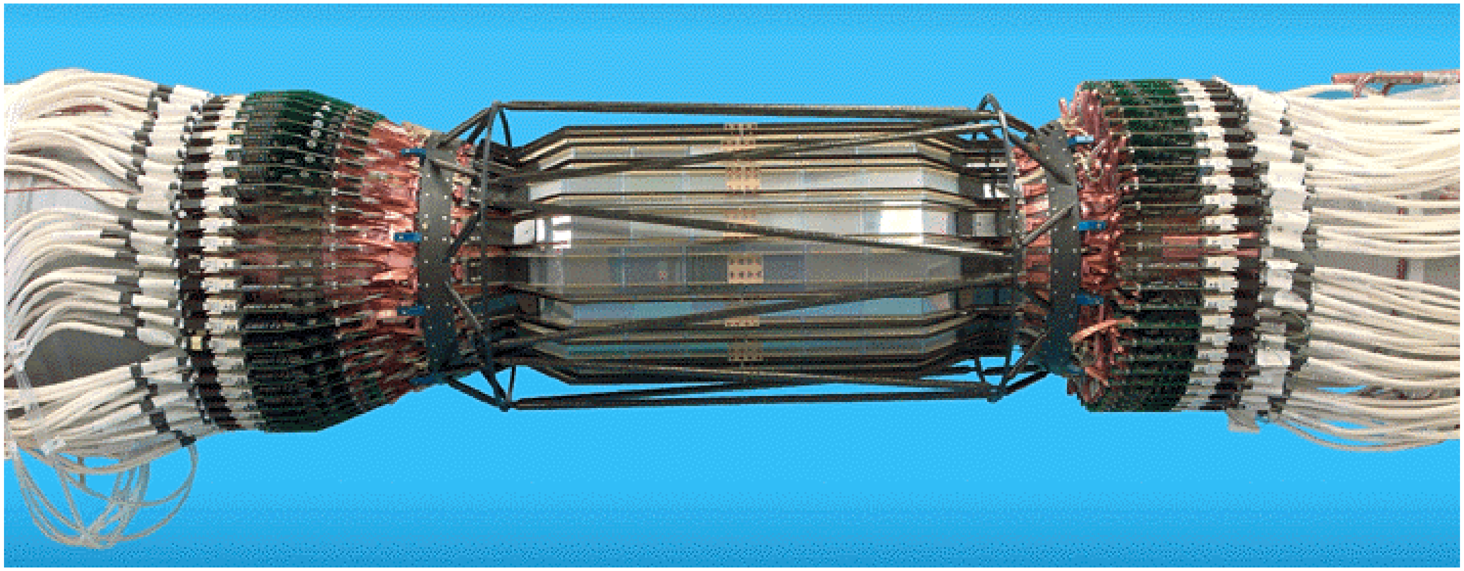


The BaBar Silicon Vertex Tracker (SVT)

Claudio Campagnari
University of California
Santa Barbara

Outline

- Requirements
- Detector Description
- Performance
- Radiation

SVT Design Requirements and Constraints (from TDR)

Performance Requirements

- Δz resolution < 130 mm
- Single vertex resolution < 80 mm.
- Stand-alone tracking for $P_T < 100$ MeV/c.

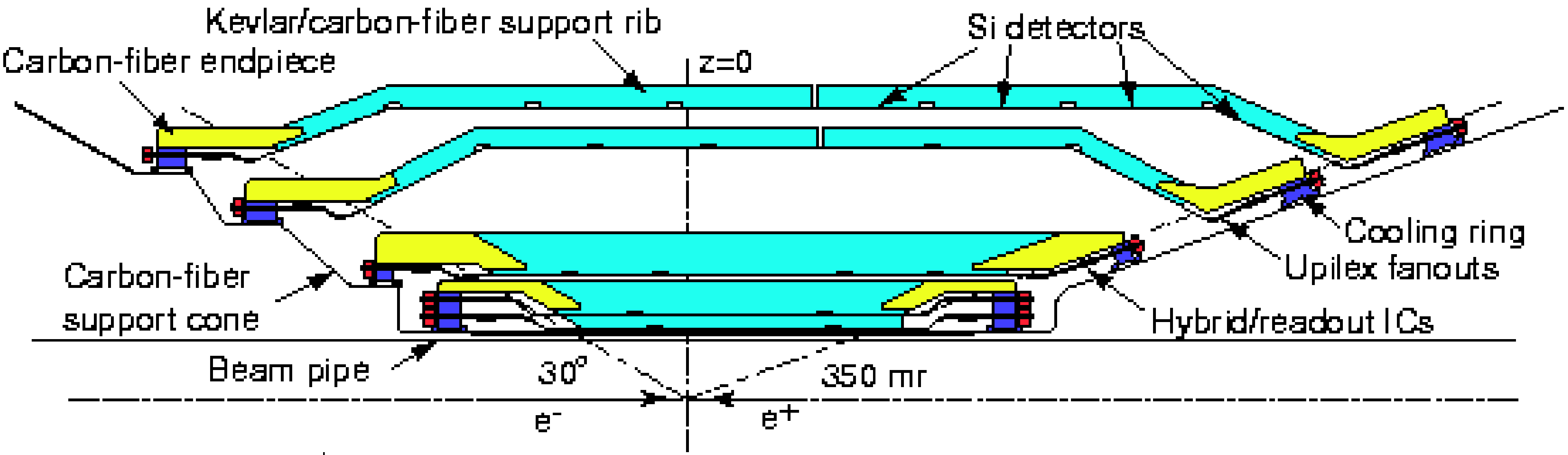
PEP-II Constraints

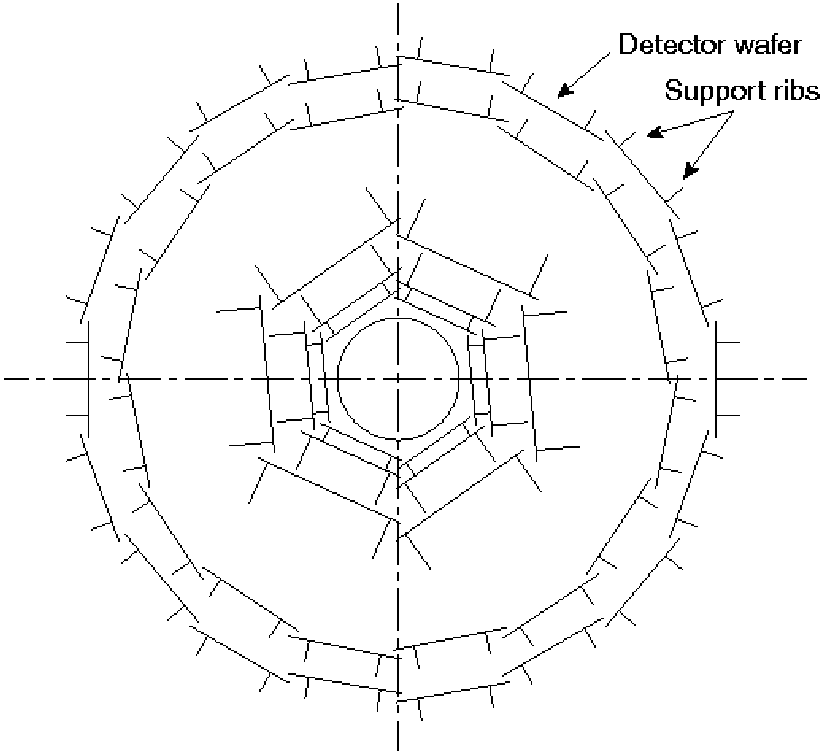
- Permanent dipole (B1) magnets at +/- 20 cm from IP.
  - Polar angle restriction: $17.2^0 < \Theta < 150^0$.
  - Must be clam-shelled into place after installation of B1 magnets
- Bunch crossing period: 4.2 ns (nearly continuous interactions).
- Radiation exposure at innermost layer (nominal background level):
  - Average: 33 kRad/year.
  - In beam plane: 240 kRad/year.
- SVT is designed to function in up to 10 X nominal background.

SVT characteristics

- Five layers, double sided
  - Barrel design, L4 and 5 not cylindrical
  - 340 wafers, 6 different types
  - Low mass Kevlar-Carbon Fiber support ribs
- Upilex fanouts to route signal to ends
- Double-sided AlN HDI (104 of these)
  - Outside tracking volume
  - Mounted on Carbon Fiber cones (on B1 magnets)
- Atom chips
  - 1156 chips, 140K channels

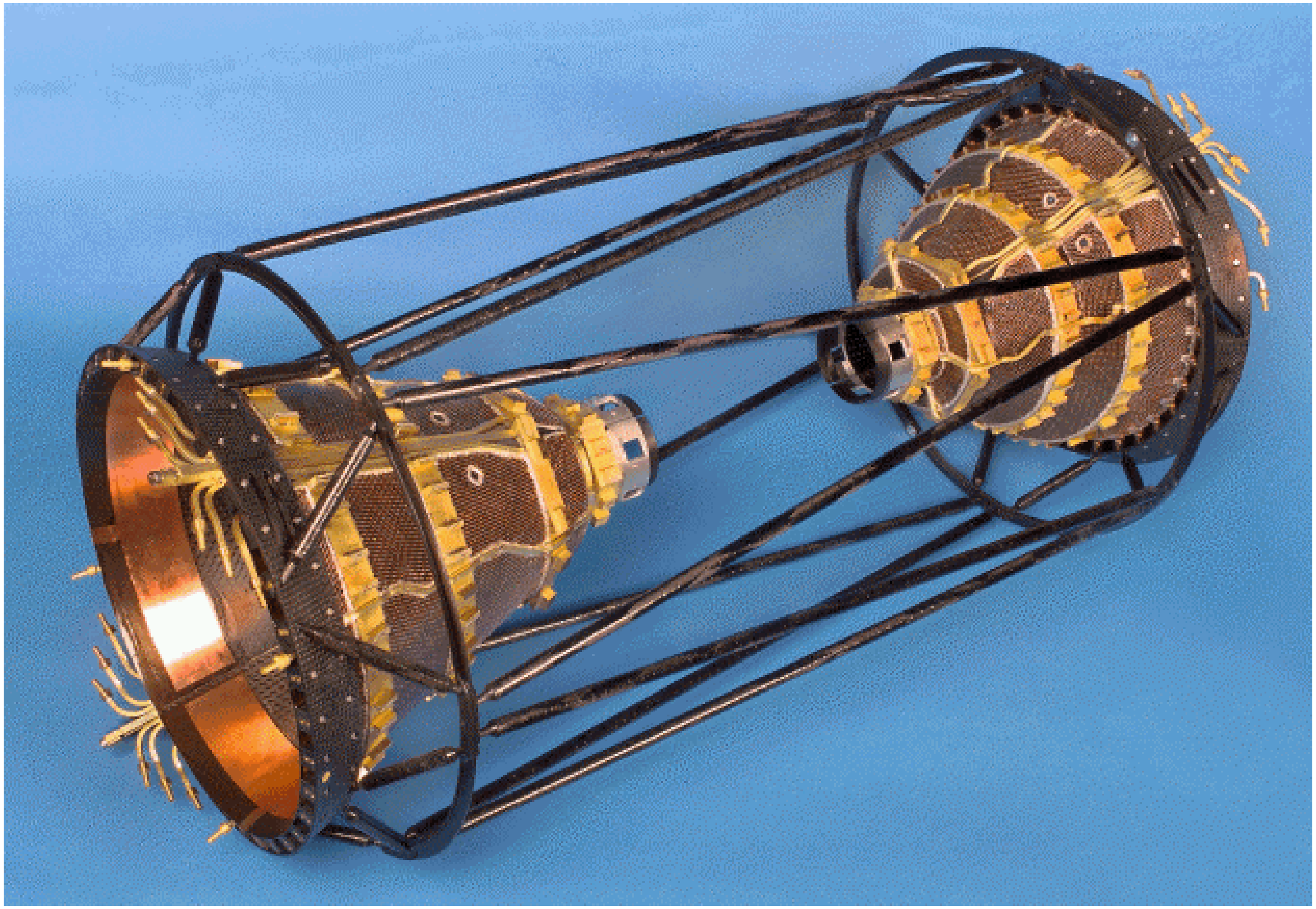
BaBar Silicon Vertex Tracker



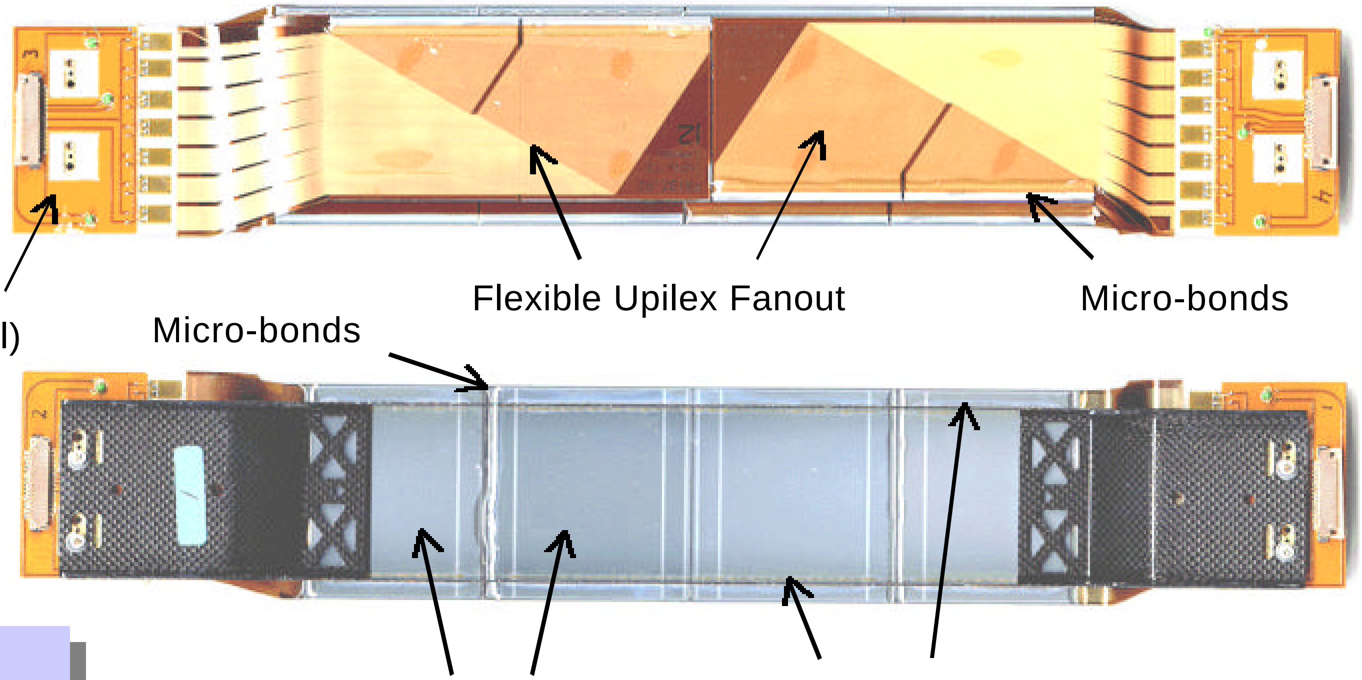


Layer	Radius (mm)	Modules/ Layer	Wafers/ Module	F Pitch (mm)	Z Pitch (mm)
1	32	6	4	50 or 100	100
2	40	6	4	55 or 110	100
3	54	6	6	55 or 110	100
4a	124	8	7	100	210
4b	127	8	7	100	210
5a	140	9	8	100	210
5b	144	9	8	100	210

Space Frame and Support Cones…mounted on B1 magnets



SVT Modules



Z-Side

High Density
Interconnect
(mechanical model)

Flexible Upilex Fanout

Micro-bonds

Micro-bonds

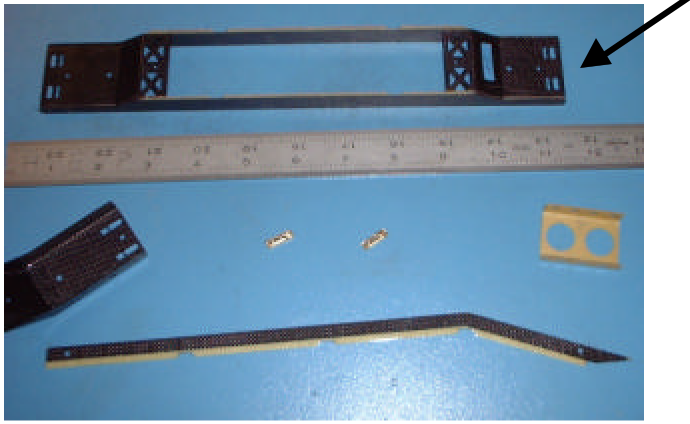
Phi-Side

Si Wafers

Carbon/Kevlar fiber
Support ribs

Fanout Properties:

- < 0.03 % X_0
- 0.52 pF/cm



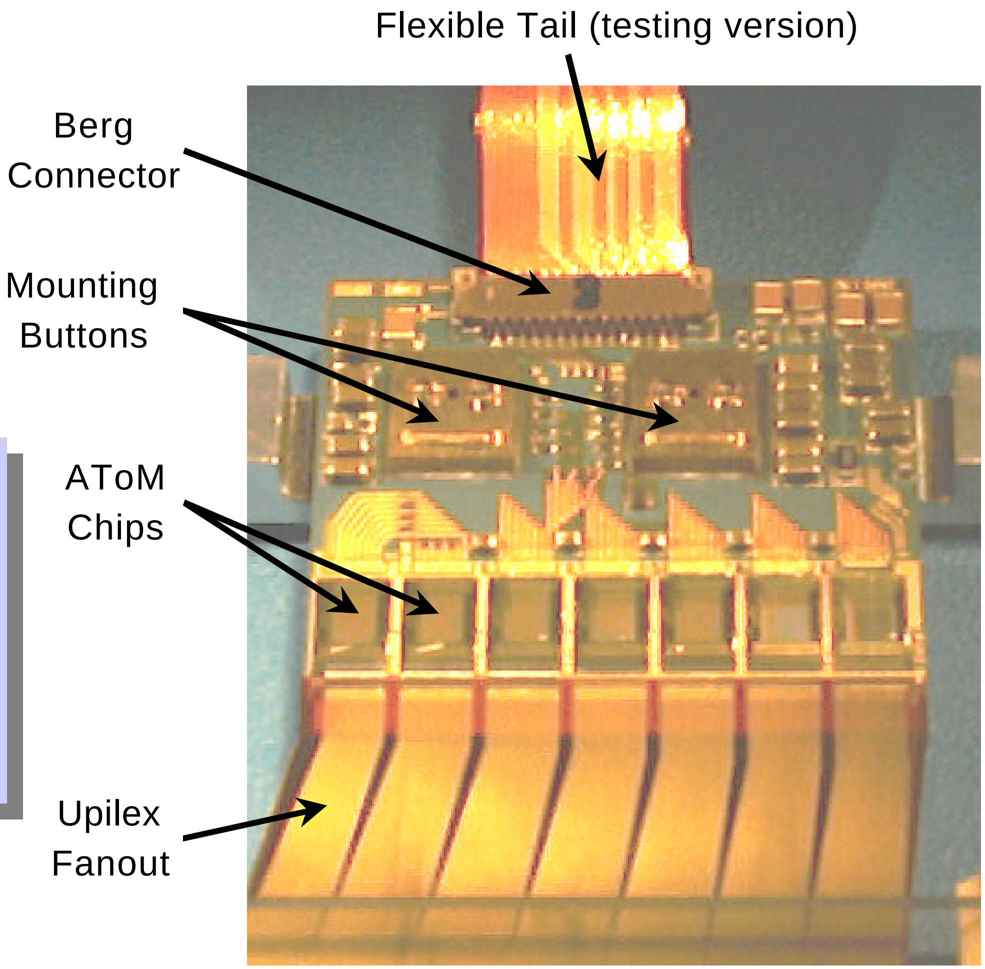
SVT High Density Interconnect

Functions:

- Mounting and cooling for readout ICs.
- Mechanical mounting point for module.

Features:

- AlN substrate.
- Double sided.
- Thermistor for temp. monitor.
- 3 different models.



Silicon Wafers

Features

- Manufactured at Micron.
- 300 µm thick.
- 6 different wafer designs.
- n^- bulk, 4-8 kΩ cm.
- AC coupling to strip implants.
- Polysilicon Bias resistors on wafer, 5 MΩ.

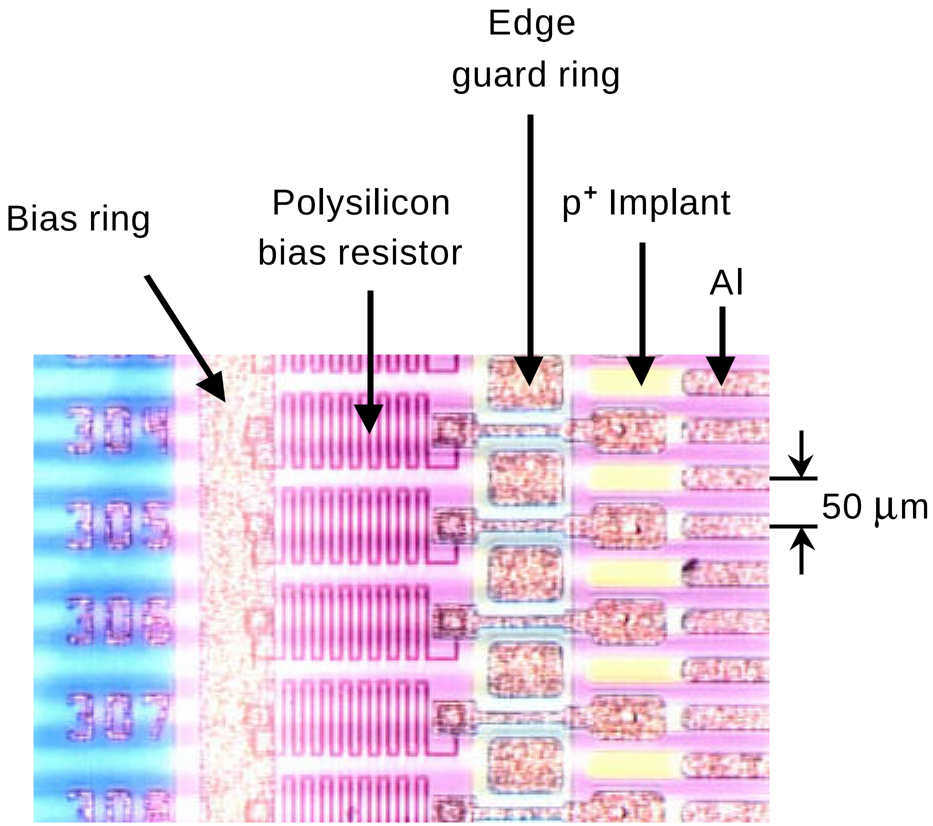
Bulk Properties

- **Bias current:** 0.1 to 2.0 µA
- **Bulk current:** 0.1 to 2.0 µA
- **Depletion voltage:** 10 to 45 V

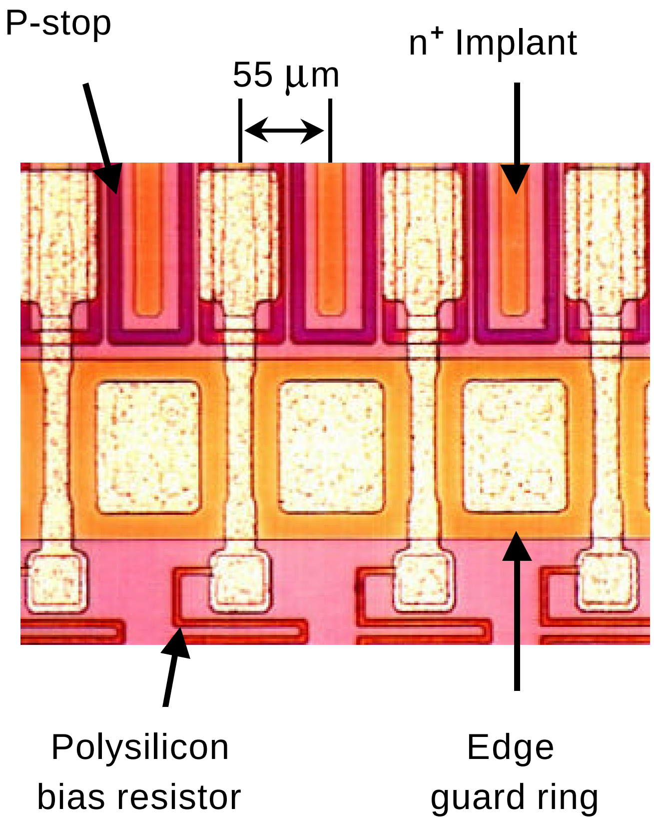
Strip Properties

	n-side	n-side	n-side	p-side
• **Strip Pitch:**	50 µm	55 µm	105 µm	50 µm
• **Inter-strip C:**	1.1 pF/cm	1.0 pF/cm	1.0 pF/cm	1.1 pF/cm
• **AC decoupling C:**	20 pF/cm	22 pF/cm	34 pF/cm	43 pF/cm
• **Implant-to-back C:**		0.19 pF/cm	0.36 pF/cm	0.17 pF/cm
• **Bias R:**	4 to 8 MΩ	4 to 8 MΩ	4 to 8 MΩ	4 to 8 MΩ

Silicon Wafers



p^+ strip side

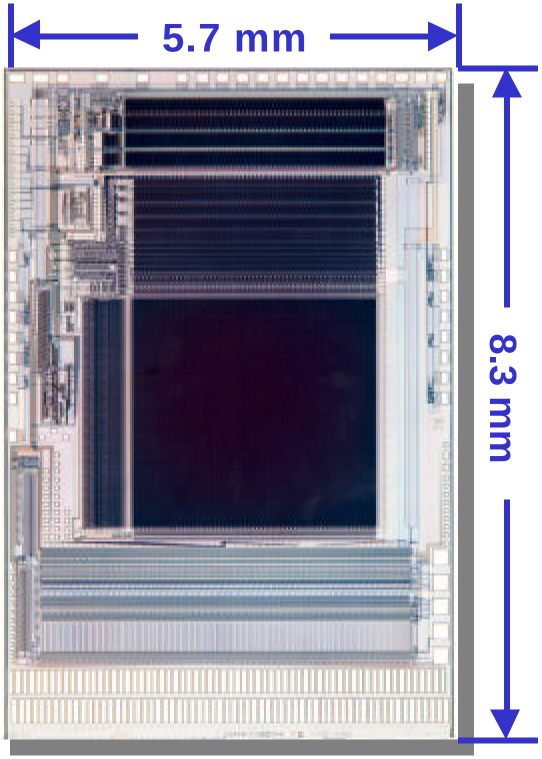


n^+ strip side

The AToM Chip

Custom Si readout IC

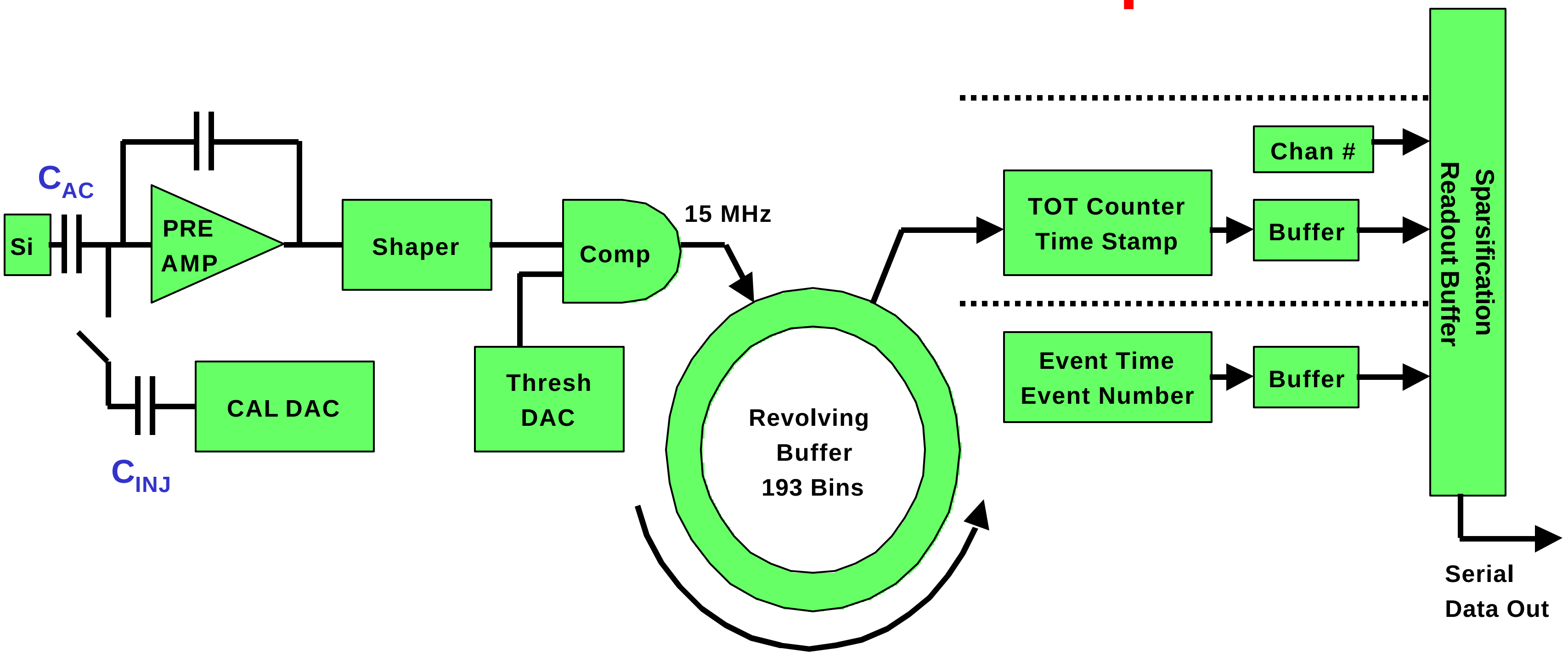
AToM = **A** **T**ime **O**ver threshold **M**achine



Features:

- 128 Channels per chip
- Rad-Hard CMOS process (Honeywell)
- Simultaneous
  - Acquisition
  - Digitization
  - Readout
- Sparsified readout
- Time Over Threshold (TOT) readout
- Internal charge injection

The AToM Chip



Amp, Shape, Discr, Calib

- 5-bit CAL DAC (0.5 fC/count)
- 5-bit Thr DAC (0.05 fC/count)
- Shaping time 100 - 400 ns
- Typical threshold 0.6-0.9 fC

Trigger Latency Buffer

- 15 MHz Sample rate
- Total storage = 12.7 us

TOT, Tstamp, Buffering

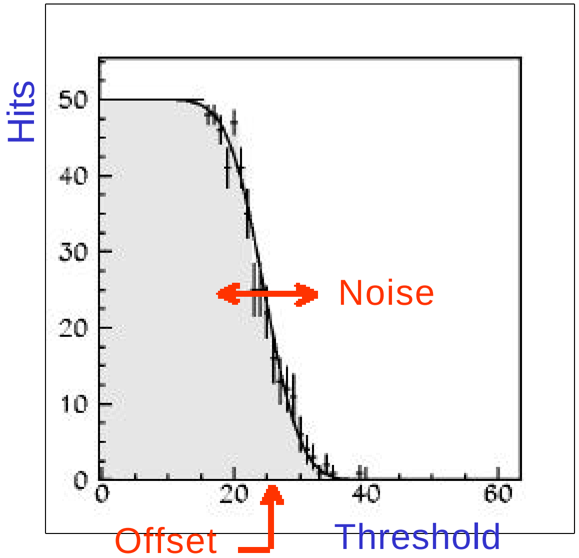
- 4 bits TOT (logarithmic)
- 5 bits Hit Tstamp
  (67 ns/count)
- 4 buffers / channel

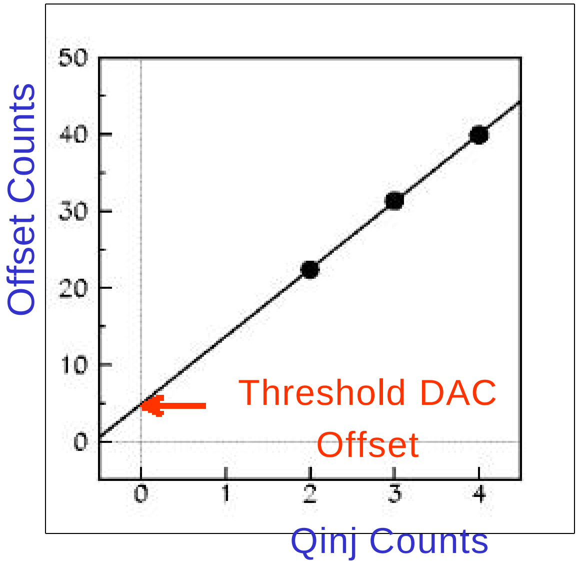
Performance

- Calibration, Noise
- Occupancy
- Efficiency
- Intrinsic Resolution

Calibration

- Noise, gain, pedestals, bad channels obtained from scanning threshold with and without charge injection and counting hits
  - 600K errfun fits, 150K linear fits
  - once a day; takes ~ 2 minutes
- Very stable
- Downloadable chip parameters have not changed since Oct 1999



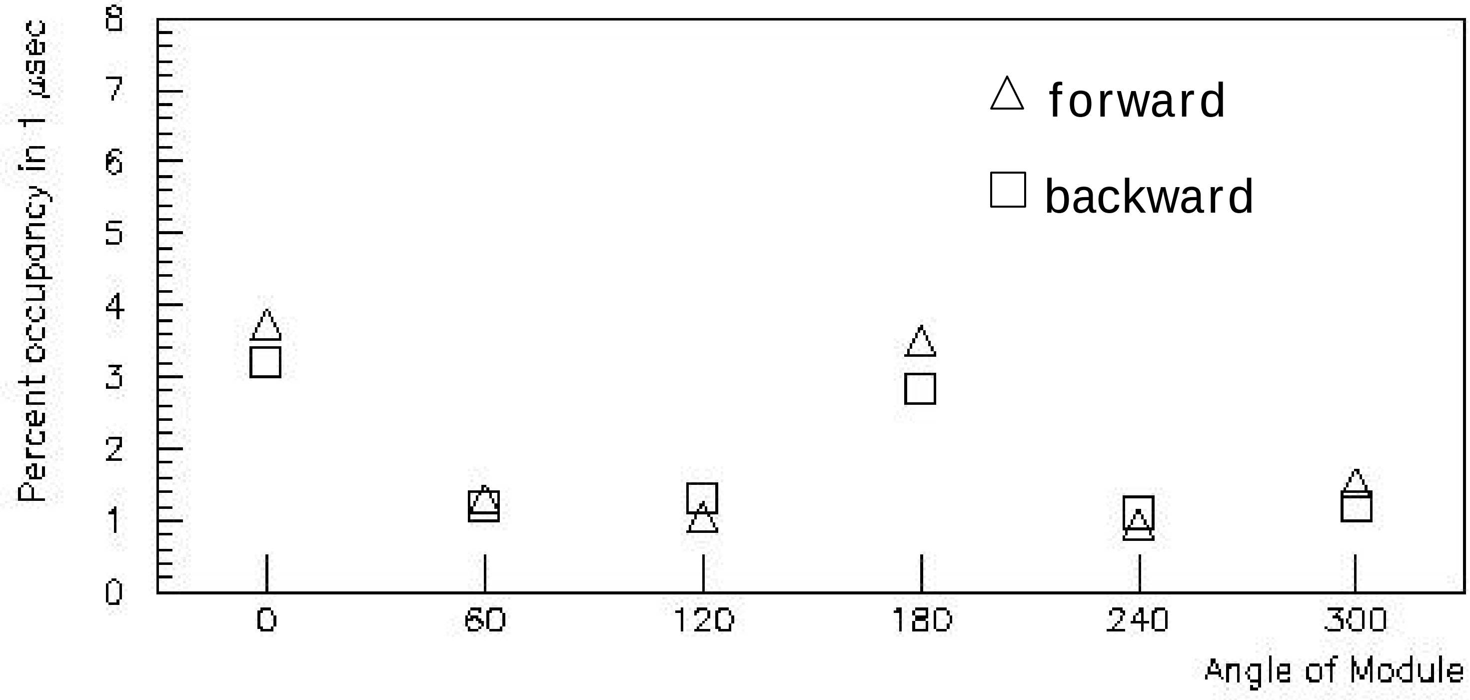


Noise

Layer	**ENC**	**Layer**	**ENC**
1ϕ	1200	1z	880
2ϕ	1240	2z	970
3ϕ	1440	3z	1180
4ϕ	1350	4z	1210
5ϕ	1600	5z	1200

1 MIP at normal incidence, about 23,000 electrons

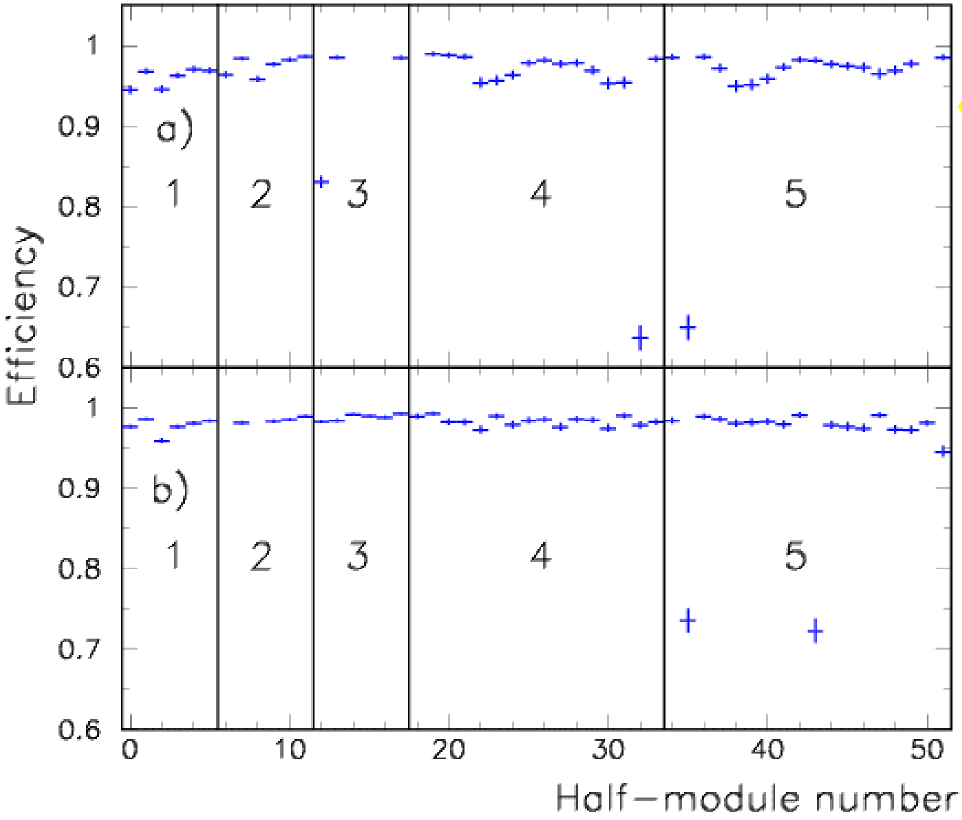
Occupancy (Layer 1)



Offline Δt ~ 300 nsec

→ effective occupancy lower by factor ~ 3

Cluster efficiency

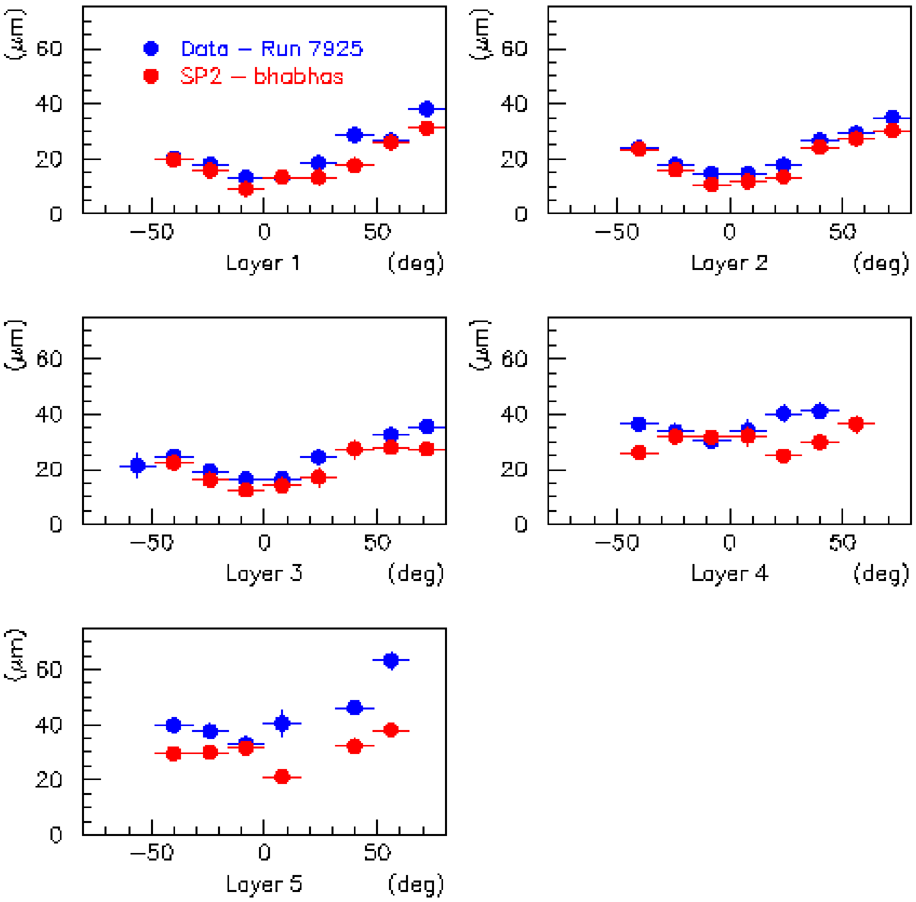


$\varepsilon \sim 97\%$
(SW + HW)

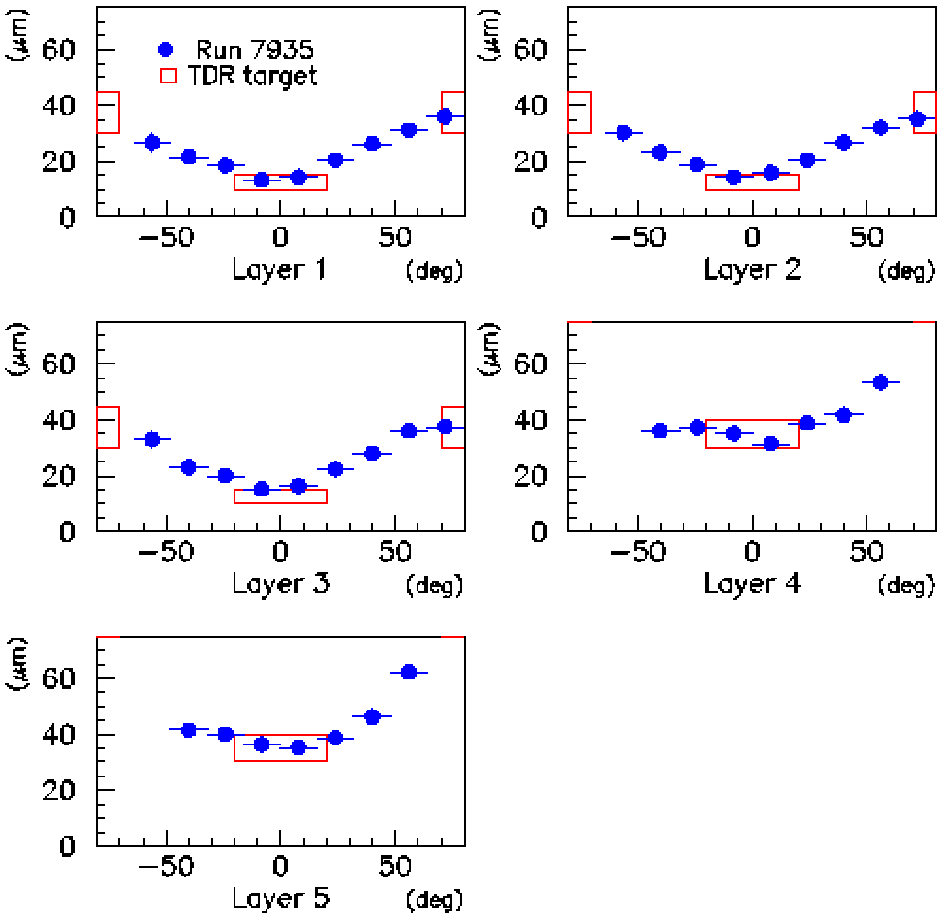
Excluding 9/208
malfunctioning readout sections

Resolution

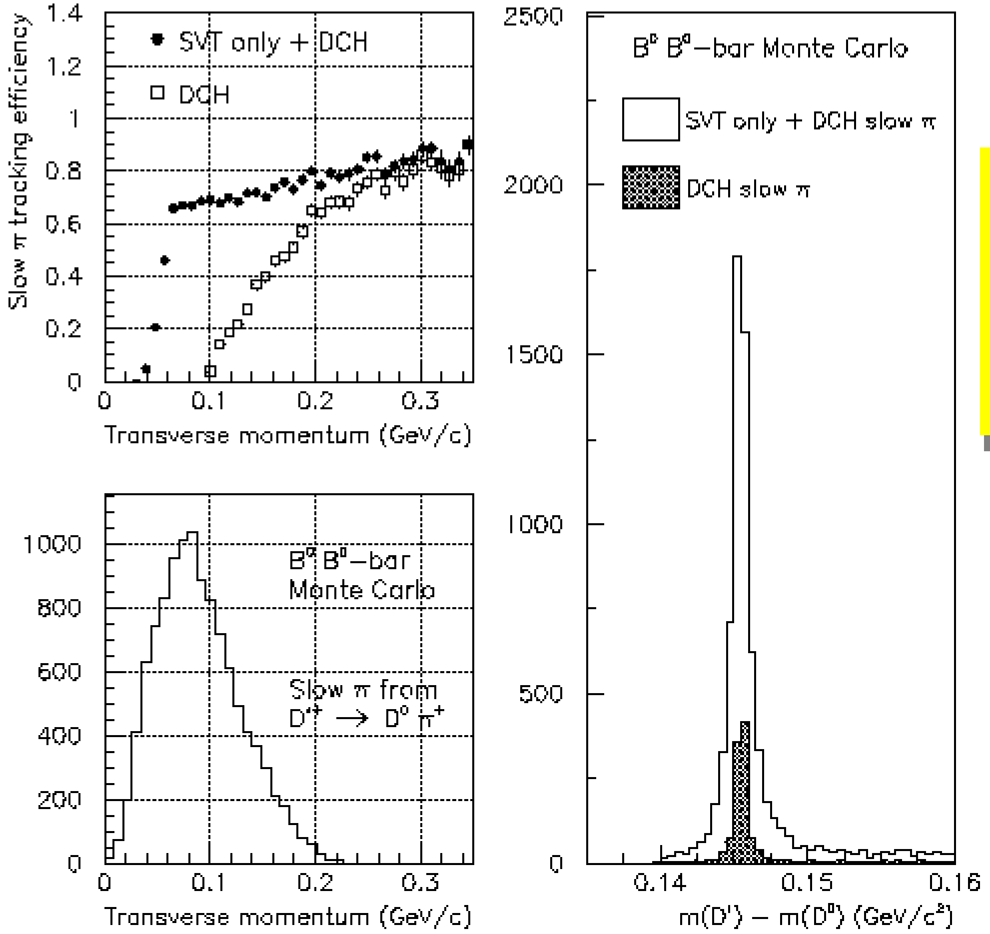
Resolution vs projected angle -Zed



SVT Hit Resolution vs Angle - Zed View



Standalone reconstruction of low P_T tracks



Reconstruction of π_s from

$D^* \to D\,\pi_s$

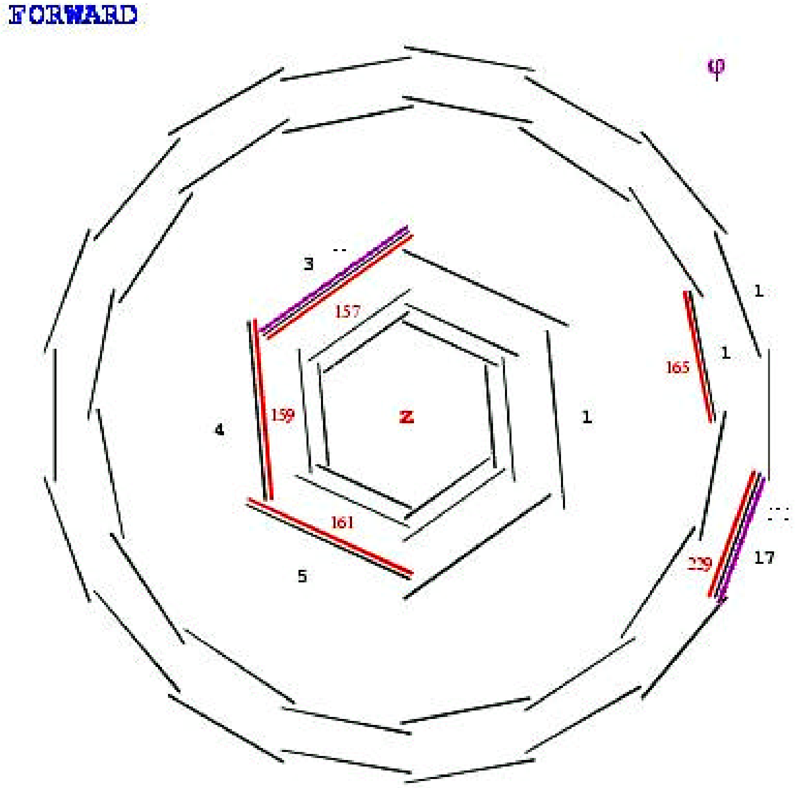
is (mostly) with SVT alone

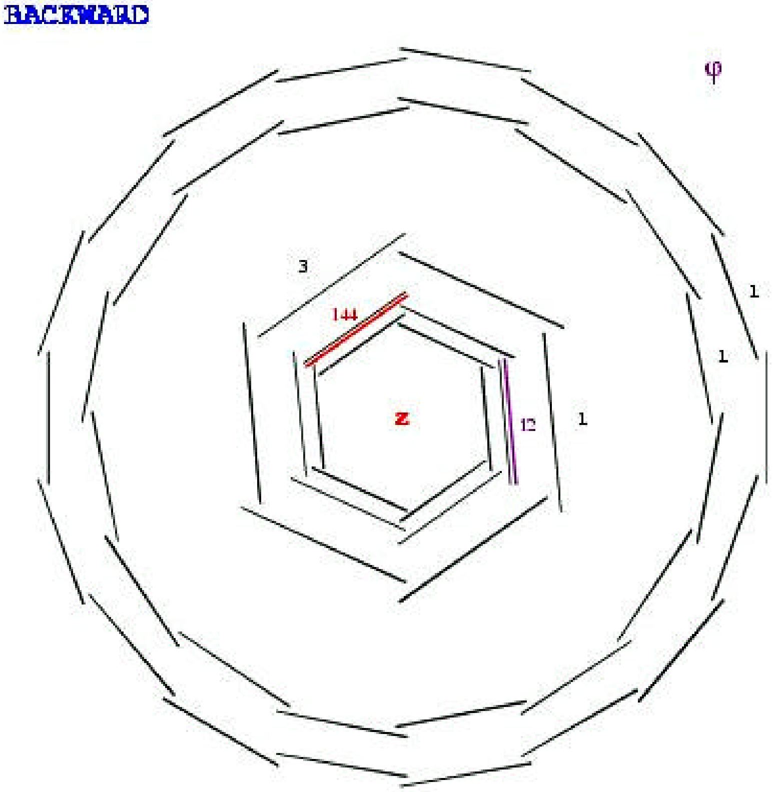
Map of malfunctioning modules (9/208)

- Layer 1 perfect
- Problems are from
  - shorts on hybrids
  - elec. probems on wafers
  - slipped out cables

— Bad ϕ

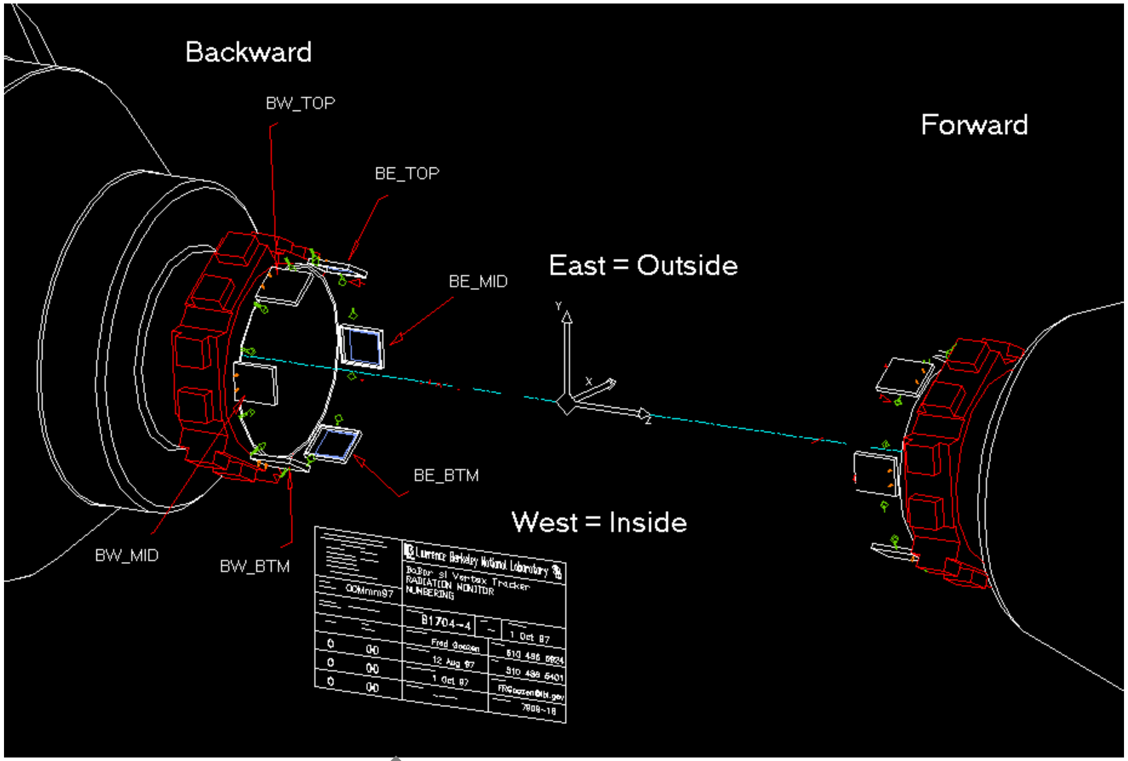
— Bad z





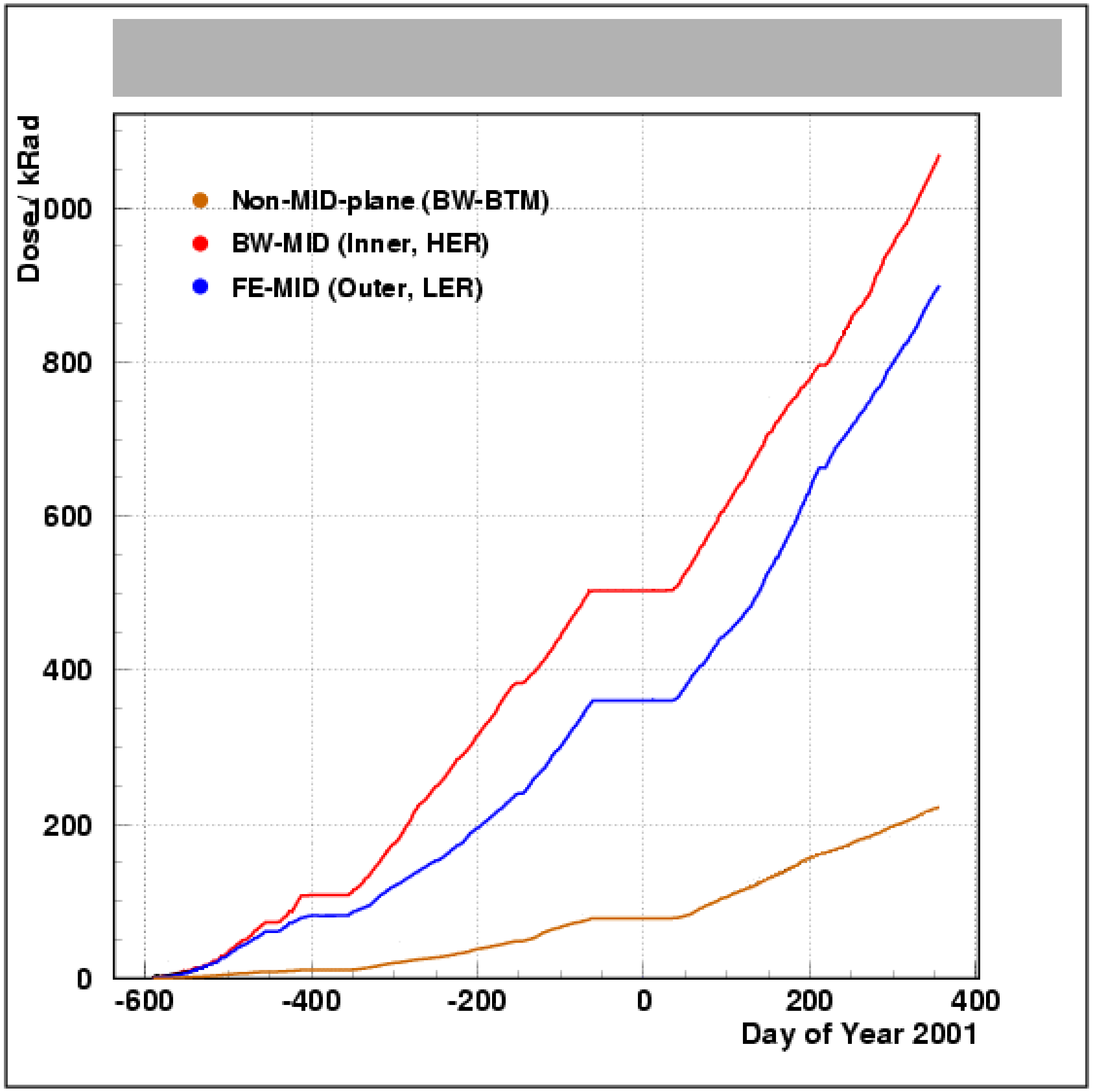
Radiation

- Monitored by 12 diodes at ~ radius of layer 1
- Diodes can abort beam
- Operation tricky due to heavy radiation damage



SVTRAD System

Measured absorbed Dose



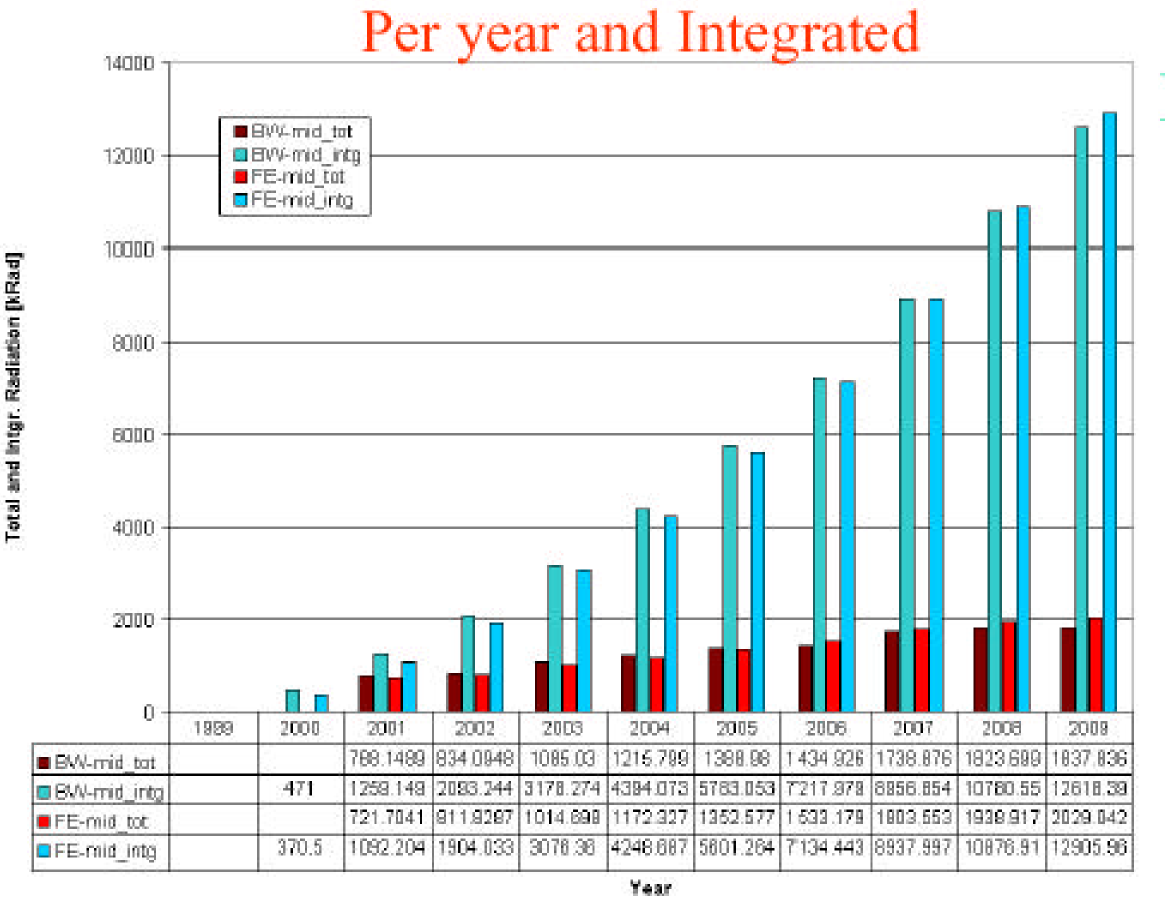
Projected absorbed dose, midplane

Based on PEP II current profile and measured dose/current

Includes injection, etc

A bit conservative….

Off-midplane ~ x5 lower


Per year and Integrated

	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009
BW-mid_tot			788.1489	834.0948	1085.03	1215.799	1388.98	1434.926	1738.876	1823.699	1837.836
BW-mid_intg		471	1259.149	2093.244	3178.274	4394.073	5783.053	7217.978	8956.854	10780.55	12618.39
FE-mid_tot			721.7041	811.8297	1014.898	1172.327	1352.577	1533.179	1803.553	1938.917	2029.042
FE-mid_intg		370.5	1092.204	1904.033	3078.38	4248.687	5601.264	7134.443	8937.997	10876.91	12905.96

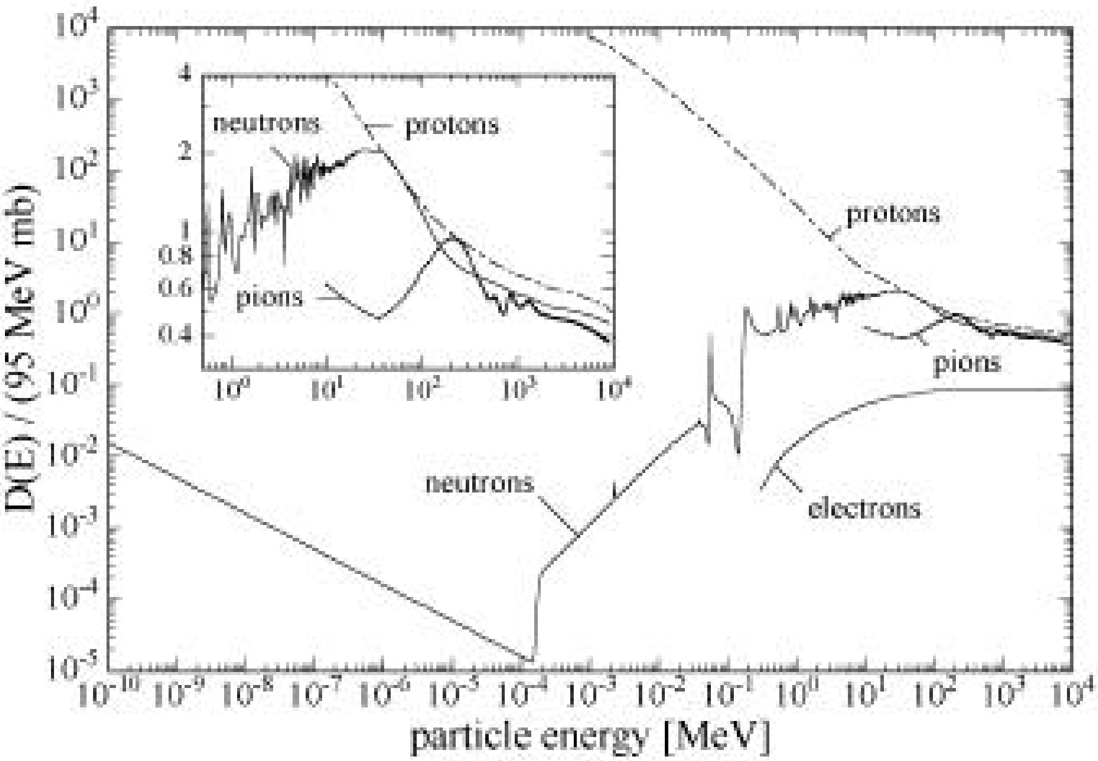
Consequences of high doses

- Bulk damage to Si
  - increase I_{LEAK} → increase in noise
    - not a real problem until very high doses
  - type inversion
- Damage to chips
  - originally tested (fully) only to 2 MRad

  → test to higher doses

Bulk Damage

~ Damage effectiveness →

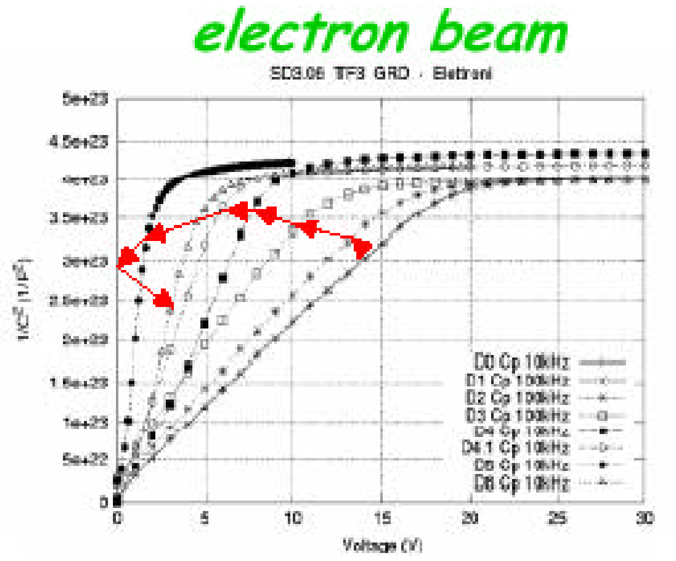


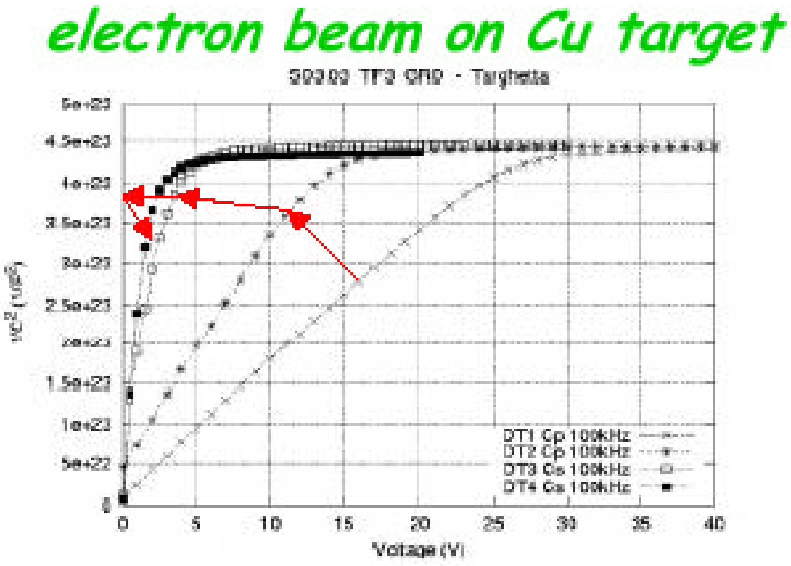
from Moll

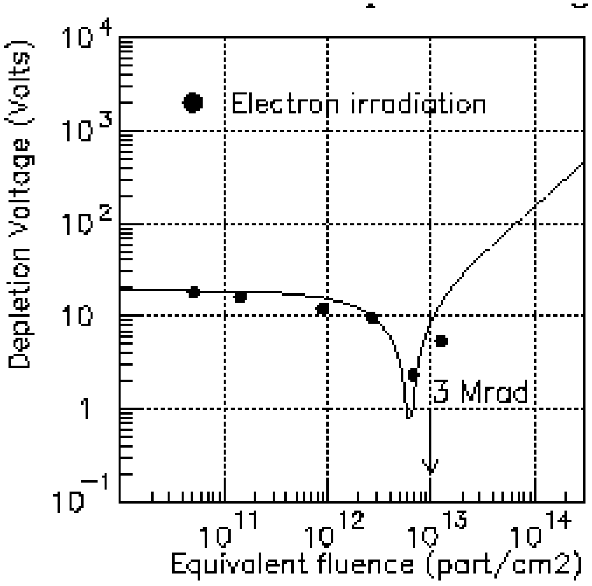
NIEL scaling: high energy electron cause significant damage (~1/10 of hadrons)

Not appreciated by us until recently

Tests at Elettra (Trieste)







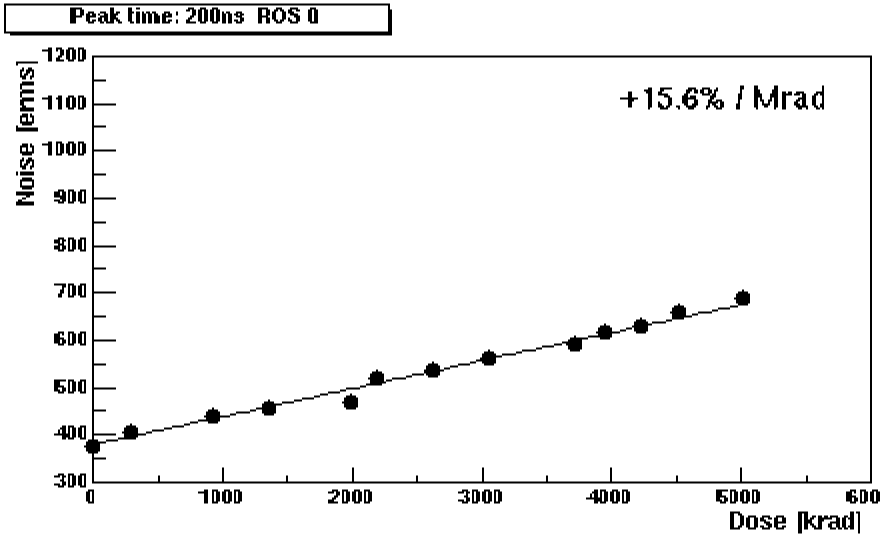
- C^{-2} vs V curve show inversion
- Results in ~ agreement with NIEL scaling hypothesis
- Leakage current increase of order 2 $\mu A/cm^2$
    - agrees with in-situ measurement

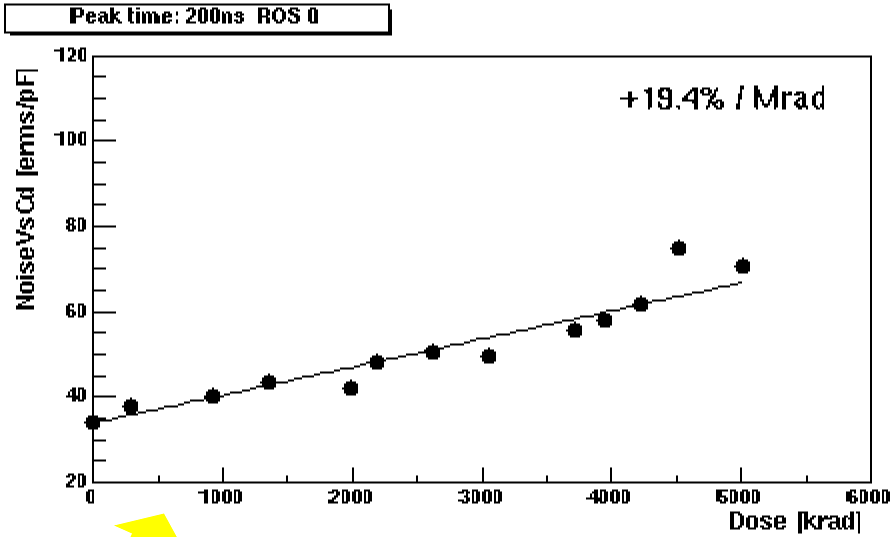
Detector Radiation Tests (Cont.)

- Electrical properties after inversion:
  - Strip isolation OK
  - Edge currents, no sudden increase, manageable
- Still to do: test of charge-collection efficiency
  - According to literature, should be OK

→ sensors OK to at least 5-6 MRad

AtoM tests beyond 2MRad





$$\text{Noise} = \alpha + \beta\, C_{\text{Load}}$$

Significant increase in noise but chip functions to at least 5 MRad

SVT Module Replacement

- Summer 04 shutdown: replace
  - L1/2 midplane modules
    - worst case dose by then ~ 3.5 MRad
  - other malfunctioning modules
- New modules identical to existing ones
- New modules under construction now

Conclusion

- The BaBar SVT is working well
    - efficient
    - resolution according to spec
    - standalone tracking
- Replace radiation damaged modules in 04
- Extend lifetime to ~ 07
- After that ?
    - depends on many things (machine, physics etc.)